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MINIMIZING POWER DISSIPATION THROUGHTRANSITION ACTIVITY

Ajay Shrivastava, Abinash Kumar

PG Scholar, EED, Dr. APJ Abdul Kalam University Indore, M.P., India

Assistant Professor, EED, Dr. APJ Abdul Kalam University Indore, M.P., India

ABSTRACT

The wide spread of handy electronic devices and the advances in VLSItechnology have enabled the implementation of complex digital circuits in asingle chip. Digital circuits consist of several interconnected logic gateswhich together perform logical operations with many input signals. In recentyears, in deep submicron and low-power VLSI design, power dissipation, andarea havebecomecriticalparameters.

Themaincauseofpowerdissipationisduetothe charginganddischarging ofinternalnodecapacitanceduring transitionactivity.Powerdissipation is the most critical parameter in handheld and mobile devices. It isclassified into two types namely static or leakage power dissipation and activeor dynamic power dissipation. Static power dissipation is caused by leakagecurrent and other static components. Dynamic power dissipation is caused bythe charginganddischargingofinter-nodecapacitance.

Inatypicalchip10%ofpowerisconsumedbystaticpowerdissipation and 90% of power is consumed by dynamic power dissipation. Asstatic power dissipated in nanowatts, only dynamic power dissipation isconsidered here. The research analyzes an efficient method to transmit huge data through interconnect with reduced transition activity,area,and powerdissipation.

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INTRODUCTION

The most important aspect of Moore's Law is that it has become a universal predictor for the growth of the entire semiconductor industry. From Moore's law, it is understood that the performance of an IC doubles every 18 months. This will increase the number of transistors used and hence increase the area and power

consumption of the circuit. In general small areas and high performances are two conflicting constraints. The IC designer's activities have been involved in trading of these constraints as shown in Figure 1.1.

Recently power dissipation is becoming an important constraint in the design process. That Low power design is becoming a new era in VLSI technology, as it impacts many applications. With the increase in speed, mobility, and miniaturization of electronic devices, the power consumption of these devices has become a major design factor. Especially for mobile devices the power consumption determines the battery lifetime. Therefore the designers, consumers, as well as environmental considerations demand a reduction of power dissipation in digital circuits. Digital circuits consist of several interconnected logic gates which together perform a function on one or more input signals. Every time an input signal changes it propagates via the gates causing a signal transition in every place where the signals propagate. This causes current to charge or discharge the capacitive load of CMOS gates which results in power dissipation

OBJECTIVE OF THEWORK

In this chapter, an overview of data compression, data coding and Hamming distance estimation techniques are discussed. Various lossless data compression techniques like run-length encoding, Huffman coding, arithmeticcoding, and dictionary-based compression principles are analyzed. Apart from all existing techniques, a novel technique named a simple byte compression algorithm for text data is developed for lossless compression. To encode the data several encoding techniques like Bus invert coding, Shift invert method, A2BC, Beach solution, gray coding, universal rotate, MDSMBC, and NBCMEI coding techniques are analyzed and a novel coding method called multi coding technique is used to encode the entire data. During data transmission,Hamming distance estimator is used to estimate the transition activity. Several full adders like logic full adder, CSL, SDSL, DDCVSL, DRDL, DPL, and SDCVSL are used to implement the Hamming distance estimator to do the arithmetic functions. Among the full adders mentioned above pass transistor logic (CPL) is used to implement the Hamming distance estimator as it takes less area and low power than other methods.

Result:-

For effective data transmission and low power consumption, it isnecessarytoknowthenumberoftransitionsthatoccurineachcodingmethod. Hamming distance estimator is used to estimate transition activity.LogicfulladderusedintheHammingdistanceestimatortoperformarithmeticfunctionsoccupiesmoreareaandpowerconsumption.Itproduces a powerdissipation of33.25mW, delayof 23.755nsand areaoccupied 159 $\mu m^{2.}$

Complementarypasstransistorlogic(CPL)fulladderwasimplemented in the Hamming distance estimator, and the results were analyzedandcomparedwithexistingCMOSlogicfulladders,intermsofpowerdissipation, delay,area,andtransistorcount.CPLlogicfulladderoccupieslessarea110 $\mu m^{2.}$,a delay of13.04ns and power dissipationof 28.972mW.

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